REMARKS

In response to the non-final Office action mailed March 26, 2003, please consider the amendments and remarks presented herein. Reconsideration and/or further prosecution of the application is respectfully requested. Additionally, formal drawings corresponding to the drawings originally filed with the present application are being filed contemporaneously with this paper.

Applicants herein amend the specification without adding new matter (a) to correct a typographical error to change "top" to "front" which more closely corresponds to the layout shown in FIG. 1B, and (b) to shorten the abstract to comply with 37 CFR § 1.72.

Applicants appreciate the citing of Fan, US Patent 5,337,308, and allowing applicants to differentiate Fan from one or more of the embodiments disclosed in the present application. Fan has some common features, but Fan operates quite differently than at least one embodiment disclosed and claimed in the present application.

Fan is concerned with maintaining cell sequence integrity *in a switching module* and providing cells to subsequent modules to reduce empty buffer probability and allowing none of the switching modules of the second and third stages to become empty to reduce delay through the switching system. Fan col. 7, ll. 29-36, and col. 2, ll. 1-4 (*emphasis added*). Details of the operation of forwarding packets are described especially in relation to FIG. 3 and as described in col. 6, ll. 15-57 and FIGs. 5A-B and as described in col. 7, ll. 1-36.

In attempting to maintain cell sequence integrity within a switching module, Fan will generate idle cells at empty output buffers according to that of the last transferred cell within a cell time (e.g., idle cell with time stamp "t+1" in the example of FIG. 5A), thus each input of a subsequent stage will have a cell, either a data or idle cell, with a timestamp cell. Fan teaches that when all input buffers have at least one cell, the earliest timestamp of these cells is detected by minimum time stamp detector 34, which provides it to selector 35 to cause one cell with the earliest timestamp to be removed from its corresponding input and forwarded. This process is repeated n times for an n x n switching module. The example of FIGs. 5A-B further clarifies that

both the steps of determining the smallest timestamp and the sending of a cell are repeated *n* times during a cell time as cells with both timestamps t and t+1 are sent in a single cell time. Thus, Fan teaches that during a cell time for an *n* x *n* next stage switching module, the *n* cells at the input buffers having the lowest timestamps will be removed from the input buffers and will be either routed to the appropriate output buffer if it is a data cell or dropped if it is an idle RT cell.

This neither teaches nor suggest determining when no additional packets received at a given switch element input will have a source timestamp value earlier than a specified value, nor maintaining sequence within the switching system. Fan neither teaches nor suggests taking into consideration the type of cell (e.g., data cell or idle cell) in determining how many cells to forward. This is required in order to be able to determine when no additional packets received at a given switch element input will have a source timestamp value earlier than a specified value, and to maintain sequence within the switching system.

The problem with the Fan's teachings will become clear with the following example. Assume that a 4x4 switch has one cell in each of its four input buffers, with one of these cells being an idle cell with time T, and the other three being data cells with time T+2 being routed to a different output buffer. After the cell time, these four cells will be processed and each output buffers will contain a cell with a timestamp of time T+2: the routed three data cells and an idle RT cell of time T+2 (corresponding to the timestamp of the last cell sent during the cell time). After already sending one or more cells of time T+2, it is possible that a cell with timestamp of T or T+1 will subsequently arrive at the switch. Thus, Fan neither teaches nor suggests determining when no additional packets received at a given switch element input will have a source timestamp value earlier than a specified value, and Fan neither teaches nor suggests maintaining sequence within the switching system.

In contrast, the present application discloses an embodiment which distributes resquencing operations among the multiple switch elements making up the interconnection network by determining when packets passing along different paths in the network can be safely

forward (e.g., determining when no additional packets received at a given switch element input will have a source timestamp value earlier than a specified value, and forwarding only packets having a timestamp less than or equal to the specified value). Page 7, line 25 to p. 8, l. 10. The present application includes the concept of a floor indication, wherein a floor indication with a value *j* in a buffer means that any cells arriving in the future are guaranteed to have a timestamp at least as large as *j*. Page 10, ll. 6-8. Thus, as shown at least in FIGs. 3, 4, 7 and explained in page 11, lines 10-24, that when determining which cell to transmit, if the smallest timestamp is associated only with a floor indication, then processing is discontinued until the next cell time. For example, step E of FIG. 7 determines whether a cell (in contrast to a floor indication) has the earliest timestamp, and if not, processing is completed for the cell time.

Thus and in contrast to Fan, the present application teaches that for a 4x4 switching module with exactly one cell/floor indication in each of its input buffers, these four cells/indications will *not* be processed irregardless of the combination of timestamp and type of cell. For example, with one of these cells being an floor indication cell with time T, and the other three being data cells with time T+2 being routed to a different output buffer, the output buffers after the cell time will each include a floor indication of time T, with the cells with timestamp T+2 remaining in the input buffer. It is possible that a cell with timestamp of T or T+1 will subsequently arrive at the switch, but it will not matter, as no cell with a timestamp of T+2 has been forwarded. In other words, the present application teaches how to determine when no additional packets received at a given switch element input will have a source timestamp value earlier than a specified value, and how to maintain sequence within the switching system.

The following remarks reference the same numbered paragraphs of the Office action to which they are directed.

Paragraph 2. Claims 1-5, 7, 9, 11, 12, 14, 19 and 20 stand rejected under 35 USC § 102(b) as being anticipated by Fan, US Patent 5,337,308.

In regards to independent claim 1, claim 1 recites the element of "determining when no additional packets received at a given switch element input will have a source timestamp value earlier than a specified value," which is neither taught nor suggested by Fan. First, the Office action fails to provide a rejection for this element as required by the MPEP, rather the Office action describes the operation of Fan without indicating what corresponds to this element (and other elements). Next, as previously discussed herein, Fan's use of idle RT cells and earliest timestamp detection does not, and neither teaches nor suggests how to determine when no additional packets received at a given switch element input will have a source timestamp value earlier than a specified value. For at least these reasons, claim 1 is believed to be allowable.

In regards to dependent claims 2-4 , these are believed to be allowable for at least the same reasons as for their independent claim 1, and thus these particular rejections are moot. Applicants do however reserve the right to further address these rejections should these particular rejections become no longer moot in the future. Moreover, Fan neither teaches nor suggests claim 3's sensing a status message establishing a lower bound on the source timestamp values of the additional packets for at least the same reasons as Fan's mechanism does not, and neither teaches nor suggests how to determine a lower bound of later arriving packets as previously discussed herein.

In regards to independent claim 5, claim 5 recites the element of "means for sensing when no subsequent packets which enter each of the plurality of arrival buffers will have a source timestamp having a value earlier than a specified value," which is neither taught nor suggested by Fan. As previously discussed herein, Fan's use of idle RT cells and earliest timestamp detection does not, and neither teaches nor suggests how to sense when no subsequent packets which enter each of the plurality of arrival buffers will have a source timestamp having a value earlier than a specified value. For at least these reasons, claim 5 is believed to be allowable.

In regards to dependent claims 7 and 9, these are believed to be allowable for at least the same reasons as for their independent claim 5, and thus these particular rejections are moot. Applicants do however reserve the right to further address these rejections should these particular rejections become no longer moot in the future.

In regards to independent claim 11, claim 11 recites the element of "means for sensing when no additional packets which enter each of the plurality of arrival buffers will have an individual source timestamp value earlier than a specified value," which is neither taught nor suggested by Fan. As previously discussed herein, Fan's use of idle RT cells and earliest timestamp detection does not, and neither teaches nor suggests how to sense when no additional packets which enter each of the plurality of arrival buffers will have an individual source timestamp value earlier than a specified value. For at least these reasons, claim 11 is believed to be allowable.

In regards to independent claim 12, claim 12 has been amended herein to be re-presented original claim 17 (and to correct a typographical error), and is believed to be allowable for at least the reason that Fan/Holden/Toy et al., alone or in combination, neither teaches nor suggests the limitation of the "departure status message indicating an earliest source timestamp value of any data packet that might be subsequently transmitted to the second preselected downstream neighbor element" for at least the reasons previously discussed herein. Amended claim 12 (represented claim 17) will be will also be addressed hereinafter in relation to paragraph 6.

In regards to dependent claim 14, claim 14 is believed to be allowable for at least the same reasons as for its independent claim 12, and thus this particular rejection is moot. Applicants do however reserve the right to further address this rejection should these particular rejection become no longer moot in the future.

In regards to independent claim 19, claim 19 recites the element of "control logic to recognize when no future packets received at the set of arrival buffers will indicate a source timestamp value earlier than a predetermined value," which is neither taught nor suggested by Fan. As previously discussed herein, Fan's use of idle RT cells and earliest timestamp detection does not, and neither teaches nor suggests how to recognize when no future packets received at the set of arrival buffers will indicate a source timestamp value earlier than a predetermined value. For at least these reasons, claim 19 is believed to be allowable.

In regards to dependent claim 20, claim 20 is believed to be allowable for at least the same reasons as for its independent claim 19, and thus this particular rejection is moot. Applicants do however reserve the right to further address this rejection should these particular rejection become no longer moot in the future.

Paragraph 4. Claims 6, 8, 16, and 21-23 are rejected under 35 USC § 103(a) as being unpatentable over Fan, US 5,337,308 in view of Holden, US 5,570,348. Each of dependent claims 6, 8, 16, and 21-23 are believed to be allowable for at least the reasons for allowance of their respective independent claims as presented herein, and thus these particular rejections are moot. Applicants do however reserve the right to further address these rejections should these particular rejections become no longer moot.

Paragraph 5. Claim 10 is rejected under 35 USC § 103(a) as being unpatentable over Fan, US 5,337,308 in view of Toy et al., US 4,630,260. Dependent claim 10 is believed to be allowable for at least the reasons for allowance of its independent claim 5 as presented herein, and thus this particular rejection is moot. Applicants do however reserve the right to further address this rejection should these particular rejection become no longer moot in the future.

Paragraph 6. Claims 15, 17, and 18 are rejected under 35 USC § 103(a) as being unpatentable over Fan, US 5,337,308 in view of Holden, US 5,570,348 and Toy et al., US 4,630,260.

In regards to claim 15, claim 15 is believed to be allowable for at least the same reasons as for its independent claim 12, and thus this particular rejection is moot. Applicants do however reserve the right to further address this rejection should these particular rejection become no longer moot in the future.

In regards to claim 17 and as discussed previously in relation to paragraph 2, independent claim 12 has been amended herein to become re-presented original claim 17 (and to correct a typographical error), and is believed to be allowable for at least the reason that Fan/Holden/Toy et al., alone or in combination, neither teaches nor suggests the limitation of the "departure status message indicating an earliest source timestamp value of any data packet that might be subsequently transmitted to the second preselected downstream neighbor element" for at least the reasons previously discussed herein. As such, the § 103 rejection is moot. Applicants do however reserve the right to further address this rejection should these particular rejection become no longer moot in the future.

In regards to claim 18, claim 18 has been cancelled herein for business purposes to use the claim fee for paying for a new independent claim added herein. Applicants do however reserve the right to represent independent claim 18 in this or a future application.

Paragraph 7. Claim 13 is rejected under 35 USC § 103(a) as being unpatentable over Fan, US 5,337,308 in view of Abali et al., US 5,721,820. Dependent claim 13 is believed to be allowable for at least the reasons for allowance of its independent claim 12 as presented herein, and thus this particular rejection is moot. Applicants do however reserve the right to further address this rejection should these particular rejection become no longer moot in the future.

In regards to new claims 24-33:

First, the prior art of record neither teaches nor suggests "in response to identifying that not one of said data packets has associated therewith the earliest timestamp value, discontinuing forwarding of said one or more data packets during a current cell time" recited in new independent claim 24, and means for that in new independent claim 29. Support for these elements and how the prior art of record neither teaches nor suggest these elements are previously described herein when differentiating Fan from at least one embodiment disclosed in the present application. This support includes, but is not limited to step E of FIG. 7 and FIGs. 3 and 4 , and the corresponding text. Fan teaches not to discontinue processing, but rather to continue sending packets or idle RT cells within the current cell time. For at least these reasons, independent claim 24 and its dependent claims 25-27, and independent claim 29 and its dependent claims 30-32 are believed to be allowable.

Second, the prior art of record neither teaches nor suggests "wherein said forwarding the particular data packet during the current cell time includes removing the particular data packet from an arrival buffer and if said removing causes the arrival buffer to become empty, in response adding a new floor indication to the arrival buffer" recited in new independent claim 28, and means for that in new independent claim 33. Support for these elements and how the prior art of record neither teaches nor suggest these elements are previously described herein when differentiating Fan from at least one embodiment disclosed in the present application. This support includes, but is not limited to step G of FIG. 7 and FIGs. 3 and 4 , and the corresponding text. Fan teaches to provide idle RT cells at the output, and provides no teaching to add an idle RT cell to an input buffer when it becomes empty during a cell time. For at least these reasons, independent claims 28 and 33 are believed to be allowable.

CONCLUSION

In view of the above remarks, the application is considered in good and proper form for allowance, and the Examiner is respectfully requested to pass this application to issue. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

The Commissioner is hereby generally authorized under 37 C.F.R. § 1.136(a)(3) to treat this communication or any future communication in this or any related application filed pursuant to 37 C.F.R. § 1.53 requiring an extension of time as incorporating a request therefore, and the Commissioner is hereby specifically authorized to charge Deposit Account No. 501430 for any fee that may be due in connection with such a request for an extension of time. Moreover, the Commissioner is hereby authorized to charge payment of any fee due any under 37 C.F.R. §§ 1.16 and § 1.17 associated with this communication or any future communication in this or any related application filed pursuant to 37 C.F.R. § 1.53 or credit any overpayment to Deposit Account No. 501430.

Respectfully submitted,
The Law Office of Kirk D. Williams

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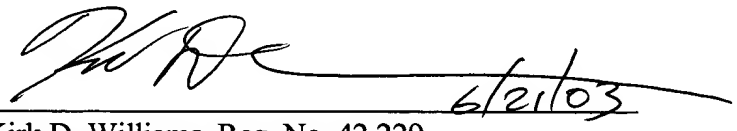
By  6/21/03

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